# IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

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1. (original) A graphics processing method, comprising the steps of:

(a.) performing 3D-graphics rendering in a graphics accelerator subsystem, using a dedicated graphics memory as primary memory for rendering accelerator logic;

(b.) using a system main memory as additional memory to hold textures required by said rendering accelerator logic; and

(c.) when textures required by said rendering accelerator logic are not present in said dedicated graphics memory, then either

downloading said textures from main memory into said graphics memory, or

selectively, when commanded by a software application, allowing said accelerator logic to read textures directly from said main memory without downloading them into said graphics memory.

2. (currently amended) A graphics processing chip, comprising:

a graphics accelerator ~~chip~~ comprising rendering acceleration logic; and

software, integrated on said chip, which has a user accessible mechanism in place to do logical-to-physical mapping into a main system memory.

3. (currently amended) A graphics processing chip, comprising:

a graphics accelerator ~~chip~~ comprising rendering acceleration logic; and

a texture memory management function, integrated on said chip, which manages both texture storage in host memory and also texture storage in normal texture memory.

4. (previously presented) The method of Claim 1, wherein said accelerator logic is able to read noncontiguous textures directly from said main memory.

5. (previously presented) The chip of Claim 2, wherein said software is able to read noncontiguous textures directly from said main memory.

6. (previously presented) The chip of Claim 3, wherein said texture memory management function is able to read noncontiguous textures directly from said main memory.